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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,276	01/14/2004	Kevin L. Beaman	MI22-2475	4316

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EXAMINER	
SMOOT, STEPHEN W	
ART UNIT	PAPER NUMBER
2813	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,276	BEAMAN ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36-41,43-45 and 49-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *36-41,49-58 and 62-65* is/are allowed.

6)☒ Claim(s) *43-45 and 59-61* is/are rejected.

7)☒ Claim(s) *66-68* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-21-06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to applicant's amendment filed on 21 November 2006.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holloway (US 6,040,249) in view of Kachelmeier (US 5,897,354 from applicant's IDS filed on 02 June 2006).

Referring to column 2, line 51 to column 3, line 9, Holloway discloses methods of nitriding an exposed surface of a gate oxide that is formed on a silicon substrate. The nitrogen is contained in a surface region of the gate oxide and is prevented from reaching a bottom region of the gate oxide (also see column 2, lines 9-15). In a first

embodiment, the exposed gate oxide surface is nitrided with free nitrogen radicals that are remotely generated by microwave plasma. In a second embodiment, a DC bias is applied to the substrate in order to provide nitrogen ions to the exposed oxide layer. After the gate oxide nitridation step, a gate electrode is deposited. The gate electrode can be n-type or p-type (i.e. conductively doped) polysilicon (also see column 1, lines 19-30). Holloway further discloses that the gate oxide can be 4 nm (i.e. 40 angstroms) thick, that the acceptable depth range of nitrogen in the 4 nm (i.e. 40 angstroms) thick gate oxide is one monolayer (about 0.3 nm or 3 angstroms) to about 3.5 nm (i.e. 35 angstroms), and that the preferred depth from the gate oxide surface is 1 nm (i.e. 10 angstroms) (also see column 2, lines 8-20). These are limitations as set forth in claims 43-45 of the applicant's invention.

However, Holloway lacks the limitation of claim 43 of forming conductively doped amorphous silicon physically against the upper portion of the silicon dioxide containing layer.

Referring to column 3, lines 34-55, Kachelmeier teaches that alternative gate materials to highly doped polysilicon include highly doped amorphous silicon.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Holloway and Kachelmeier in order to substitute amorphous silicon, as taught by Kachelmeier, for the polysilicon gate material of Holloway, because Kachelmeier recognizes that amorphous silicon is a suitable alternative gate electrode material to polysilicon (see column 3, lines 34-55).

3. Claims 59-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holloway (US 6,040,249) and Kachelmeier (US 5,897,354 from applicant's IDS filed on 02 June 2006) as applied to claim 43 above, and further in view of Noble et al. (US 6,450,116 B1).

As shown above, the combination of Holloway and Kachelmeier has all of the limitations as set forth in claim 43 of the applicant's invention. However, this combination does not expressly teach or suggest that the nitrogen species change energy states before the exposing step, which is the further limitation to claim 43 as set forth in claim 59 of the applicant's invention. More specifically, this combination does not expressly teach or suggest that the nitrogen species change from a high energy state to a lower energy state, which is the further limitation to claim 59 as set forth in claim 60 of the applicant's invention.

Referring to Fig. 3A, column 6, line 51 to column 9, line 15, and column 18, lines 1-15, Noble et al. teach a remote plasma apparatus for exposing a silicon dioxide layer on a silicon substrate to nitrogen radicals (i.e. neutral atoms occupying a high energy state – see column 8, lines 65-66). Noble et al. disclose the generation of plasma in a remote plasma applicator (300) that has a length of 12 inches and delivery of the plasma to a chamber (213) that includes the silicon substrate (100) via an inlet member (360) that has a length of 2.25 inches (see column 18, lines 1-15). The generated plasma includes nitrogen ions, nitrogen radicals, and electrons (see column 8, line 62 to column 9, line 15). The applicant's specification indicates that by separating the plasma from the substrate by a length of at least 12 inches, the highly activated nitrogen

species will inherently relax before they reach the substrate (see page 8, line 19 to page 9, line 5). Further, the disclosure of Noble et al. indicates that the nitrogen radicals have a lifetime, which implies relaxation from a high energy state to a lower energy state (see column 16, line 63 to column 17, line 30).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Holloway, Kachelmeier, and Noble et al. in order to use the plasma applicator of Noble et al. that features forming nitrogen radicals remotely at a distance of more than 12 inches from the substrate. Noble et al. recognize that there are numerous advantages for using their remote plasma applicator to form nitrogen radicals for the subsequent nitridation of an oxide, which include the formation of an effective nitride barrier at the oxide surface, rapid formation of the barrier layer, and improved device performance (see column 20, lines 7-22).

4. Claim 61 is rejected under 35 U.S.C. 103(a) as being unpatentable over Holloway (US 6,040,249) and Kachelmeier (US 5,897,354 from applicant's IDS filed on 02 June 2006) as applied to claim 43 above, and further in view of Koyama et al. (US 5,981,366).

As shown above, the combination of Holloway and Kachelmeier has all of the limitations as set forth in claim 43 of the applicant's invention. However, this combination lacks the further limitation to claim 43 as set forth in claim 61, which is forming a silicide layer over the conductively doped amorphous silicon. Koyama et al.

teach a method of forming a gate electrode that includes first depositing a phosphorus doped polysilicon layer (5) and then depositing a tungsten silicide layer (6) (see Fig. 4 and column 3, lines 3-33).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the teachings of Holloway and Kachelmeier by combining a tungsten silicide layer, as taught by Koyama et al., with the amorphous silicon gate electrode of Holloway and Kachelmeier. Koyama et al. recognize that the inclusion of tungsten silicide advantageously reduces the specific resistance of the gate electrode (see column 4, lines 14-18).

Allowable Subject Matter

5. Claims 36-41, 49-58, 62-65 are allowed.

6. Claims 66-68 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

- Claims 36-41, 56-58 are allowed because the prior art of record does not teach or suggest, in combination with the other claim limitations, a method of forming a

structure over a semiconductor substrate that includes the step of exposing a silicon dioxide containing layer to an activated nitrogen species formed from plasma conditions to provide nitrogen within the silicon dioxide containing layer, wherein substantially all nitrogen within the silicon dioxide containing layer is spaced from the substrate, combined with the subsequent steps of forming a first silicon layer physically against the silicon dioxide containing layer and a second silicon layer over the first silicon layer, wherein the first and second silicon layers comprise different conductivity types;

- Claims 49-55, 62-65 are allowed because the prior art of record does not teach or suggest, in combination with the other claim limitations, a method of forming a structure over a semiconductor substrate that includes the steps of exposing a silicon dioxide containing layer to nitrogen atoms comprising a higher energy state than their ground state to provide nitrogen primarily within an upper surface of the silicon dioxide containing layer, wherein the silicon dioxide containing layer is formed physically against a first region of the substrate, and forming conductively doped silicon physically against the upper surface of the silicon dioxide containing layer, combined with the subsequent step of oxidizing the conductively doped silicon and an exposed second region of the substrate;
- Claim 66 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a method of forming a structure over a semiconductor substrate that includes the step of exposing a silicon dioxide containing layer to nitrogen ions to provide nitrogen within only an

upper portion of the silicon dioxide containing layer, combined with the subsequent steps of forming conductively doped amorphous silicon physically against the upper portion of the silicon dioxide containing layer and forming conductive material over the conductively doped amorphous silicon, wherein the conductive material includes a conductivity type that is different from a conductivity type of the conductively doped amorphous silicon; and

- Claims 67-68 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a method of forming a structure over a semiconductor substrate that includes the step of exposing a silicon dioxide containing layer to nitrogen ions to provide nitrogen within only an upper portion of the silicon dioxide containing layer, combined with the subsequent steps of forming conductively doped amorphous silicon physically against the upper portion of the silicon dioxide containing layer and oxidizing the conductively doped amorphous silicon.

Response to Arguments

8. Applicant's arguments filed on 21 November 2006 have been fully considered but they are not persuasive.

The applicant contends that a benefit or advantage is required for combining or modifying references. However, the appropriate standard is merely a reasonable expectation for success, which is established by the teachings of Kachelmeier who

recognizes that highly doped amorphous silicon can be used as a gate electrode material (see column 3, lines 34-36 and also see column 12, lines 22-25, 49-54). Accordingly, Kachelmeier shows that highly doped amorphous silicon and highly doped polysilicon each have an art recognized suitability as a gate electrode material per MPEP section 2144.06 and 2144.07.

The applicant further contends that the combination of Holloway and Kachelmeier lacks a suggestion or motivation to combine the references. However, rationale for supporting a rejection under 35 USC 103(a) includes art recognized equivalents (see MPEP section 2144), and Kachelmeier shows that amorphous silicon and polysilicon are equivalent gate electrode materials, thereby meeting the requirement of suggesting that Holloway can be combined with Kachelmeier.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

sws

Stephen W. Smoot

STEPHEN W. SMOOT
PRIMARY EXAMINER